The Minimum mode of 8086 microprocessor.

- 8086 works in Minimum Mode, when MN/ ¯ MX = 1.
- Minimum Mode, 8086 is the only processor in the system. The Minimum Mode circuit of 8086 is as shown below:
- Clock is provided by the 8284 clock generator, it provides CLK, RESET and READY input to 8086.
- Address from the address bus is latched into 8282 8-bit latch. Three such latches are needed, as address bus is 20-bit. The ALE of 8086 is connected to STB of the latch. The ALE for this latch is given by 8086 itself.
- The data bus is driven through 8286 8-bit trans-receiver. Two such trans-receivers are needed, as the data bus is 16-bit. The trans-receivers are enabled through the DEN signal, while the direction of data is controlled by the DT/ ¯ R signal. ¯ DEN is connected to ¯ OE and DT/ ¯ R is connected to T. Both ¯ DEN and DT/ ¯ R are given by 8086 itself.

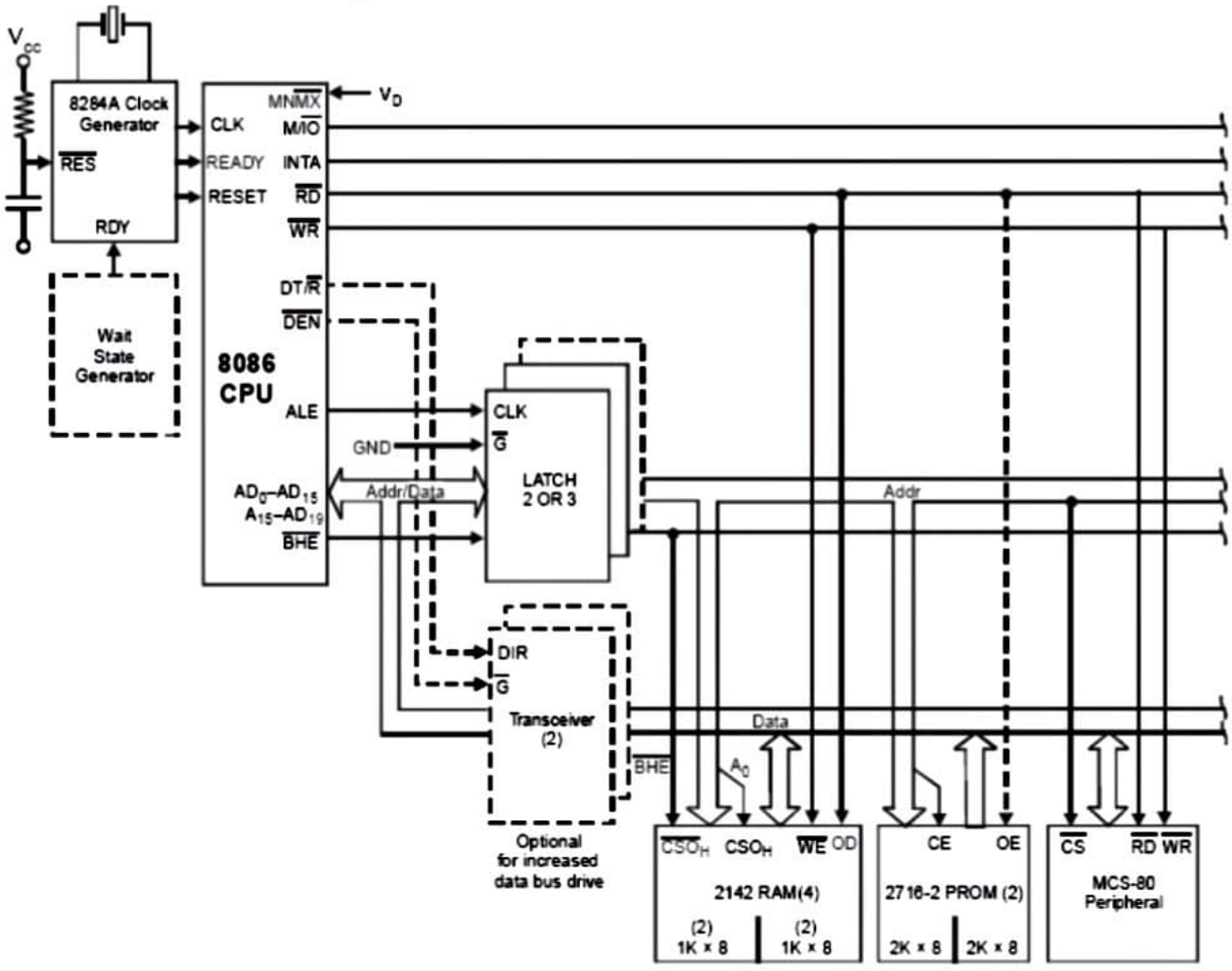
$\overline{DEN}$	DT/ $\overline{R}$	Action
1	X	Transreceiver is disabled
0	0	Receive data
0	1	Transmit data

- Control signals for all operations are generated by decoding M/ ¯ IO , ¯ RD and ¯ WR signals.

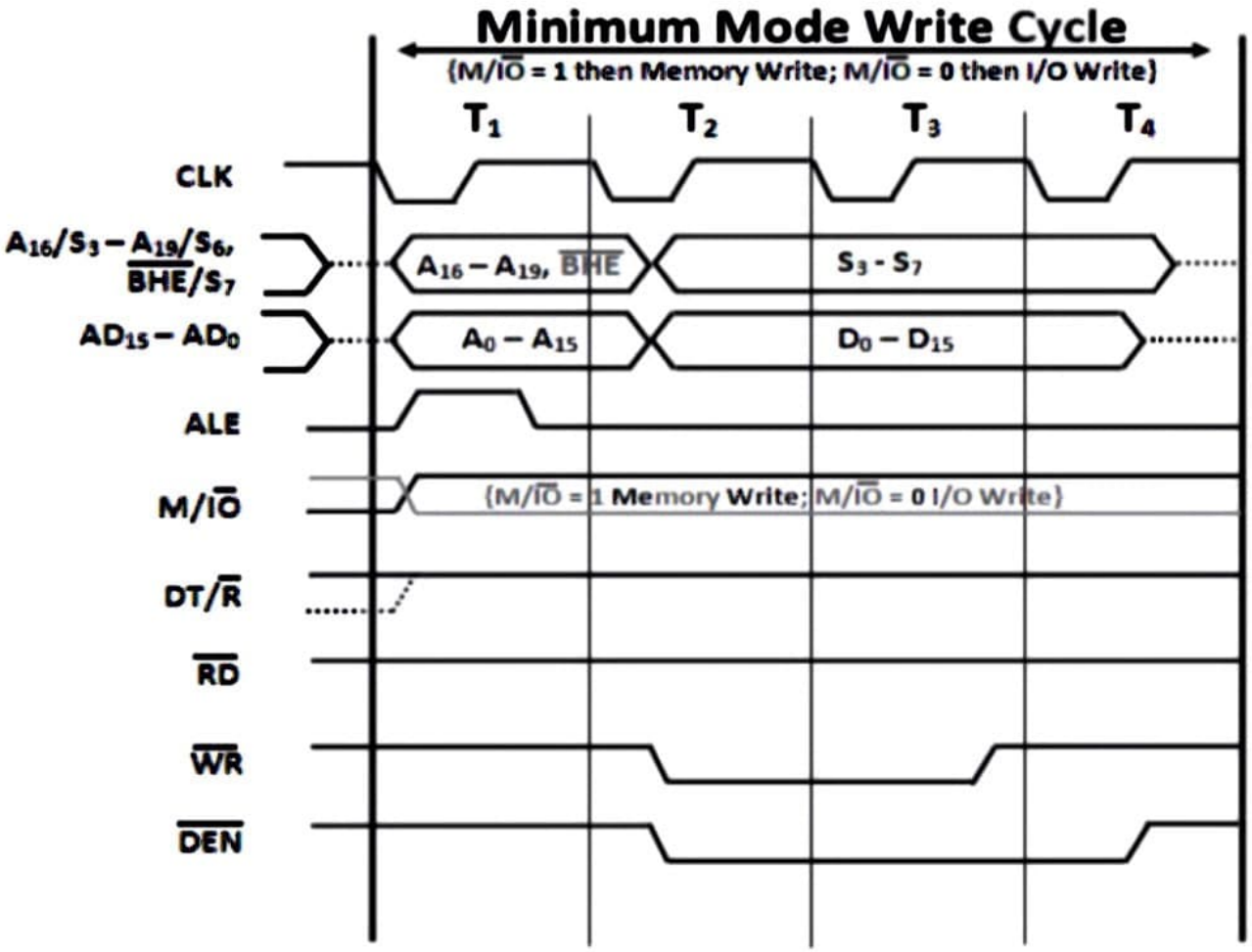
M/ $\overline{IO}$	$\overline{RD}$	$\overline{WR}$	Action
1	0	1	Memory Read
1	1	0	Memory Write
0	0	1	I/O Read
0	1	0	I/O Write

- M/ ¯ IO , ¯ RD and ¯ WR are decoded by a 3:8 decoder like IC 74138. Bus Request (DMA) is done using the HOLD and HLDA signals.
- ¯ INTA is given by 8086, in response to an interrupt on INTR line.

Minimum Mode 8086 Configuration



. **Timing diagram for write operation in minimum mode.**



Maximum Mode Configuration of 8086:

A processor is in the Maximum Mode Configuration of 8086 when its MN/MX pin is grounded. The maximum mode defines pins 24 to 31 as follows:

Pin Definitions (24 to 31) in Maximum Mode:

1. **QS_1, QS_0 (output) :** These two output signals reflect the status of the instruction queue. This status indicates the activity in the queue during the previous clock cycle.

QS_1	QS_0	Status
0	0	No operation (queue is idle)
0	1	First byte of an opcode
1	0	Queue is empty
1	1	Subsequent byte of an opcode

2. S_2,S_1,S_0 (output) : These three status signals indicate the type of transfer to be take place during the current bus cycle.

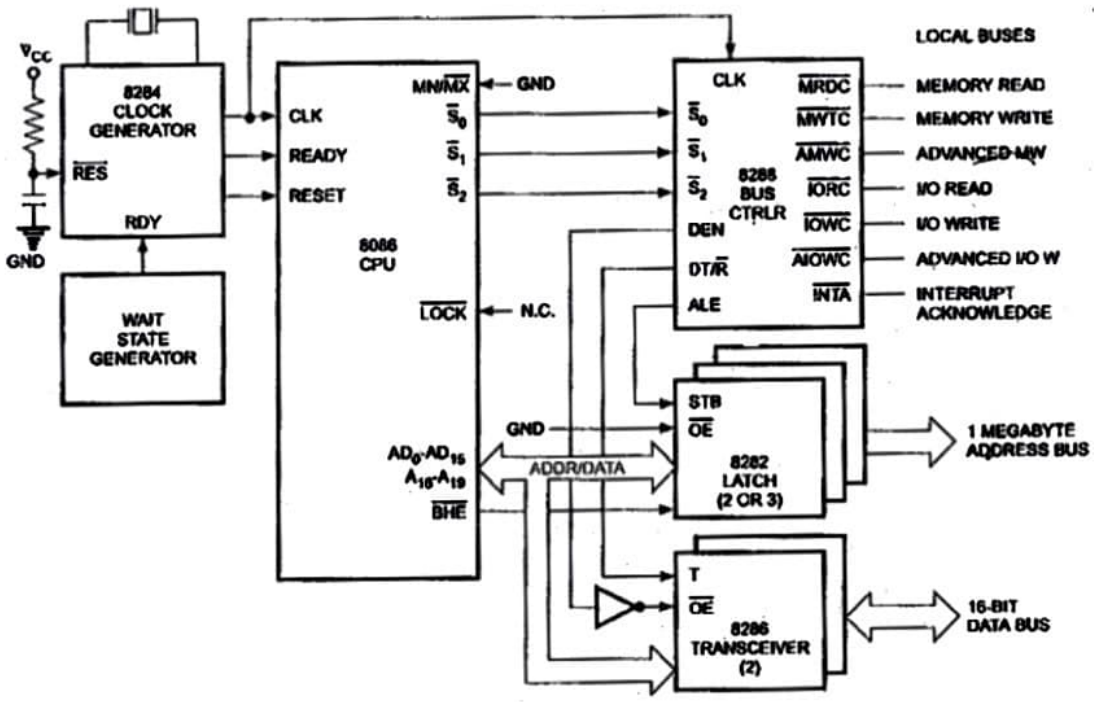
$\overline{S}_2$	$\overline{S}_1$	$\overline{S}_0$	Machine cycle
0	0	0	Interrupt Acknowledge
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt

$\overline{S}_2$	$\overline{S}_1$	$\overline{S}_0$	Machine cycle
1	0	0	Instruction fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Inactive-Passive

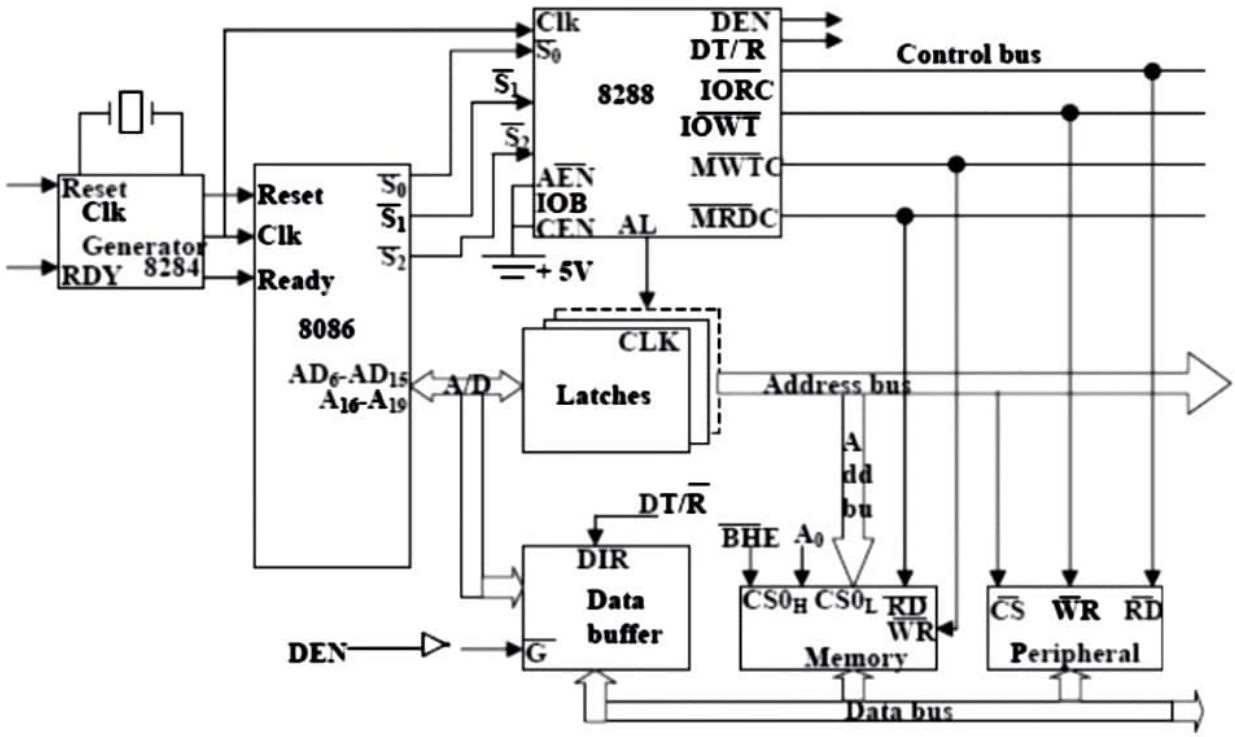
3.LOCK : This signal indicates that an instruction with a LOCK prefix is being executed and the bus is not to be used by another processor:

4.RQ/GT_1 and RQ/GT_0 : In the Maximum Mode Configuration of 8086, HOLD and HLDA pins are replaced by RQ (Bus request)/GT_0 (Bus Grant), and RQ/GT_1 signals. By using bus request signal another master, can request for the system bus and processor communicate, that the request is granted to the requesting master by using bus grantnal. Both signals are similar except the RQ/GT_0 has higher priority than RQ/GT_1.

Fig. below shows the typical Maximum Mode Configuration of 8086. In the maximum mode additional circuitry is required to translate the control signals. The additional circuitry converts the status signals (S_2-S_0) into the I/O and memory transfer signals. It also generates the control signals required to direct the data flow and for controlling 8282 latches and 8286 transceivers. The Intel 8288 bus controller is used to implement this control circuitry.



The actual Interfacing of Memory with Microprocessor-8086 in Maximum Mode is showing below:



Maximum Mode 8086 System.

Timing diagram for write operation in maximum mode.

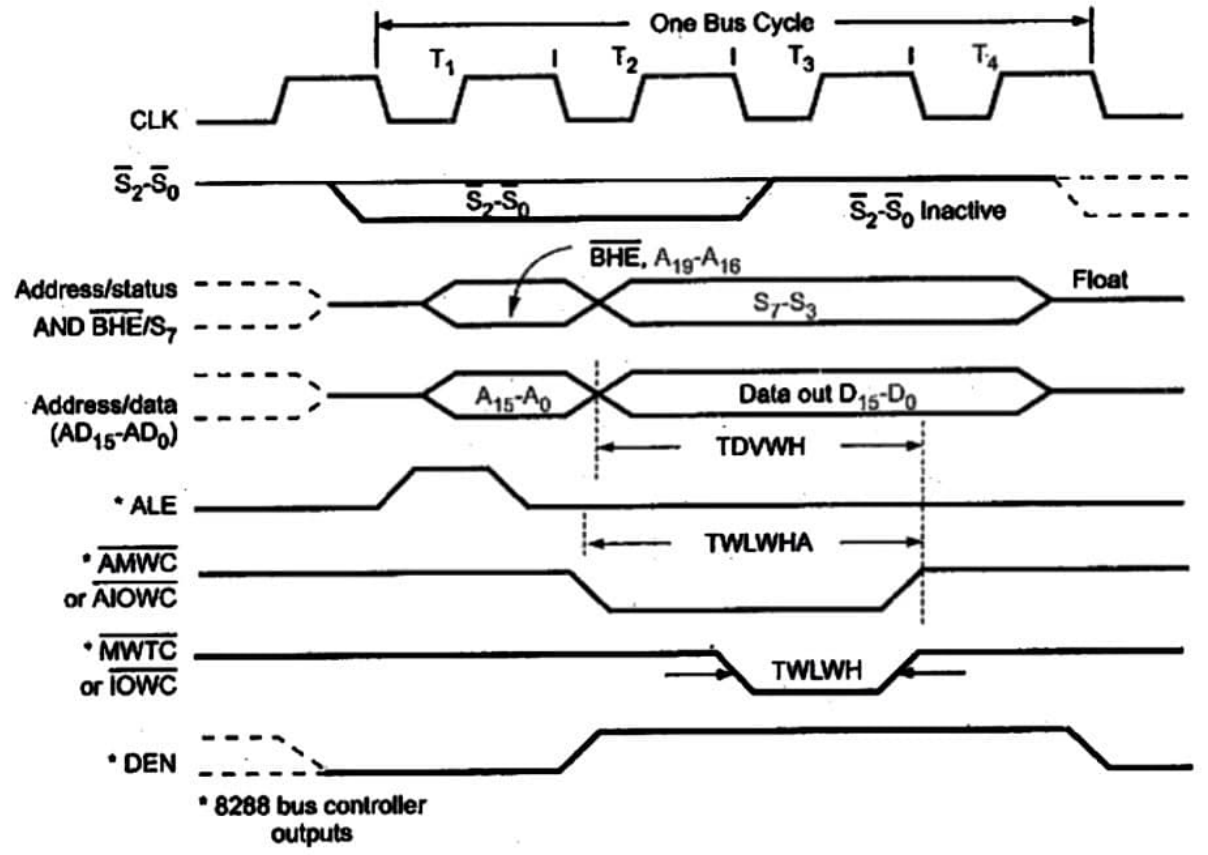


Fig. 10.10 (b) Output (write operation)